REMARKS

Claims 1 - 14 are pending in this application, of which claims 5 and 11 have been withdrawn from consideration. By this Amendment, claims 1 and 6 have been amended and new claims 12 - 14 have been added. Applicant respectfully submits that no new matter has been added. It is therefore believed that this Amendment is fully responsive to the Office Action dated January 17, 2003.

Title of the Invention:

The title of the invention has been objected to for being non-descriptive of the applicant's claimed invention. The applicants respectfully request reconsideration of this objection.

As indicated above, the title of the invention has been amended, in its entirety, so as to read as follow:

> SEMICONDUCTOR DEVICE INCLUDING AN ISLAND-LIKE DIELECTRIC MEMBER EMBEDDED IN A CONDUCTIVE PATTERN.

It is believed that such amended title of the invention is now descriptive of the claimed invention.

In view of the above, the applicant respectfully requests that the title of the invention, as submitted herewith, be approved by the Examiner, and that the outstanding objection to the title be withdrawn.

As to the Merits:

As to the merits of this case, the Examiner sets forth the following rejections:

1) claims 1 - 4, 6 and 9 - 10 stand rejected under 35 U.S.C. §102(b) as being anticipated by Jain (U.S. Patent No. 5,602,423);and

2) claims 1 - 2, 4 and 6 - 10 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hiraki (Japanese Patent Publication No. JP6-318590).

Each of these rejections are respectfully traversed.

The amended claims 1 and 6 are directed to a semiconductor device having a multilayer structure shown in Fig. 4. None of the cited references disclose the claimed semiconductor device that includes a lower conductive portion (11) formed in a lower wiring layer (10) and an upper conductive portion (31) formed in an upper wiring layer (30).

Jain shows a multilayer semiconductor device in Figs. 12 and 13. The device includes a third insulating layer 62 and a conductor 60. However, there is no disclosure of a semiconductor device having conductive portions formed in different layers. That is, Jain does not disclose an upper

conductive portion including a conductive metal and at least one dielectric member embedded in the conductive metal. Therefore, the Jain reference does not show the claimed semiconductor device.

As shown in Fig. 1 of Hiraki, insulating pillars 6 are arranged in an aperture 4 and a trench 5. As shown in Fig. 2b, the trench 5 and the aperture 4 are filled with Al-Si-Cu film 7 to form an embedded wiring 10 and a bonding pad 9, respectively. Neither the embedded wiring 10 nor the bonding pad 9 is not electrically connected to a conductive portion formed in another wiring layer. Therefore, the Hiraki reference does not show the claimed semiconductor device.

As described above, there is no disclosure of a semiconductor device having conductive portions formed in different layers in any of the applied references.

In view of the aforementioned amendments and accompanying remarks, the claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Thomas E. Brown
Attorney for Applicant
Reg. No. 44,450

TEB/kal
Atty. Docket No. **020167**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

23850
PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

Q:\FLOATERS\TEB\teb\02\020167\Amendment - April 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE 10/076,355

IN THE TITLE:

The title of the invention has been AMENDED to read as follows:

SEMICONDUCTOR DEVICE [AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE] INCLUDING AN ISLAND-LIKE DIELECTRIC MEMBER EMBEDDED IN A CONDUCTIVE PATTERN.

IN THE CLAIMS:

Claims 1 and 6 have been **AMENDED** to read as follows:

1. (AMENDED) A semiconductor device having a multilayer wiring structure, comprising:

a semiconductor substrate;

[at least one dielectric film] a lower wiring layer arranged on the substrate and having an opening[;], a conductive portion filling the opening[;], and at least one dielectric member embedded in the conductive portion [that fills the opening];

an interlayer dielectric film arranged on the lower wiring layer and having a contact wiring; and

an upper wiring layer arranged on the interlayer dielectric film and having an upper opening, an upper conductive portion filling the upper opening, and at least one dielectric member embedded in the upper conductive portion, wherein the upper wiring layer and the lower wiring layer are electrically connected by the contact wiring.

6. (AMENDED) A semiconductor device having a multilayer wiring structure, comprising:

a semiconductor substrate;

[at least one dielectric film] a lower wring layer arranged on the substrate and including an upper surface, a lower surface, [and] an opening[;], at least one dielectric member arranged in the opening[;], and a conductive portion filling the opening so as to surround the at least one dielectric member;

an interlayer dielectric film arranged on the lower wiring layer and having a contact wiring; and

an upper wiring layer arranged on the interlayer dielectric film and having an upper opening, at least one dielectric member arranged in the upper opening, and a conductive portion filling the upper opening so as to surround the at least one dielectric member, wherein the upper wiring layer and the lower wiring layer are electrically connected by the contact wiring.